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Design of Continuous Time Multibit Sigma Delta ADC for Next Generation Wireless Applications

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ABSTRACT
This paper presents the design of CT ΣΔ modulator which can provide high DR and SNR over a 20 MHz signal bandwidth. So far all the CT SDM uses either feedback or feedforward loop filter architecture. The proposed topology is a 3rd order low-pass sigma-delta modulator, which employs a combination of feedforward and feedback schemes. Loop filter is designed as RC integrators due to its high linearity and easy interface. The design starts from system level using Matlab/Simulink. Then, the first integrator in the loop, which is the most critical block in the modulator, is implemented at transistor level using Cadence Virtuoso 180 nm CMOS technology.

***Keywords* –** ADC, CMOS, Continuous Time, Sigma Delta Modulator, Dynamic Range (DR), Signal to noise ratio (SNR).

I. INTRODUCTION

Wireless receivers for next generation high bandwidth standard like LTE requires much higher ADCs with bandwidth up to 20 MHz and resolutions of 10-14 bits or better and is the key component in radio receiver [1]. Wireless applications require low power, accurate and high speed ADC's, so the evolving research toward the development of ADCs with higher speeds and higher resolutions is equally being driven by the demand of high-speed wireless communication services.

In recent years, more and more work success in both the wide bandwidth and the high resolution. There are still lots of space for improvement in continuous-time sigma-delta modulator design. When compared with the nyquist rate ADCs, oversampling ADCs offers relaxed requirements on the analog components. Most reported MHz range sigma-delta modulators are implemented using switched-capacitor (SC) [2], mainly due to mature design methodologies and robustness. The discrete-time Sigma-Delta ADC offers a good degree of accuracy. But the circuit speed is limited by the settling of switched-capacitor integrator. Recently continuous-time sigma-delta (CT ΣΔ) modulators become attractive because of its higher speed and lower power consumption characteristics. Compared with pipeline and discrete-time (DT) sigma delta converters, CT converters have advantages of a lower power consumption and inherent anti-aliasing filtering, hence extending battery life and reducing system complexity, which are especially important for portable wireless devices. Also the bandwidth requirement of operational amplifier (opamp) in CT SDM is much lower than DT SDM for a given sampling rate. Hence a third order CT SDM is chosen here. Very few wideband CT ΣΔ designed with Gm-C filters [3] but offers low SNDR and nonlinearity. In this design RC integrator is chosen for the three stages of third order loop filter [4].

The feedback architecture used in [5] suffers from integrator output swing. Thus feedforward topology suggested in [6,7]. But it still results in signal transfer function (STF) peaking. To further compensate these, a combination of both these architecture proposed in this paper.

The rest of this paper organised as follows: Section II presents the system level and circuit level design. Section III compares the CT SDM with DT SDM. Section IV concludes the paper.

II. METHOD

The design methodology and the system level design of 3rd order continuous-time sigma-delta modulator is presented here.. The top-down design flow for is shown in Figure 1. Firstly, the ADC has been designed at system level using Matlab/Simulink. High-level simulation is performed in order to count for the real circuit behaviour of the design. The modulator performance, such as desired SNDR and stability must be achieved and the specifications for every building block derived. After validating the model at behavioural level, the most critical block of the ADC was replaced by its circuit level implementation using 1.2V 180nm CMOS technology.

The design specifications are defined first. According to the specifications, initial design parameters are chosen, including sampling frequency, loop order, quantizer resolution and the DAC feedback pulse. It is then simulated in matlab/simulink and SNR plot is obtained. Finally, the building block specifications for the circuit level design are derived.

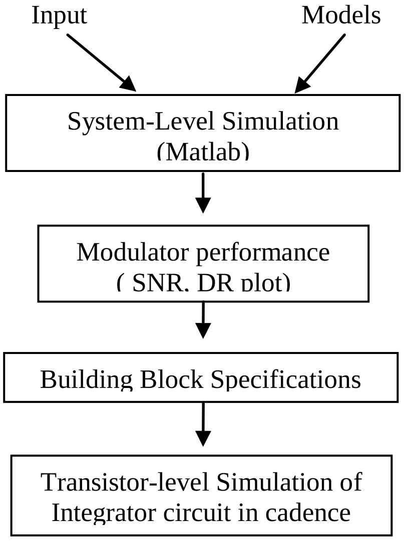


Fig. 1 Design Flow for CT SD ADC

2.1 SYSTEM LEVEL DESIGN

A sigma delta modulator typically consists of loop filter, feedforward ADC and a feedback DAC. The block diagrams of DT and CT SDM are shown in figure 2. L (Z) and L(s) represent the discrete time and continuous time loop filters respectively. The ADC usually called quantizer, converts its input to digital output. The feedback DAC converts it back to analog form and is then subtracted from input. Main characteristics of CT SD ADC are that input of CT SDM remains a CT signal, until it is sampled at quantizer. The sampling is controlled by clock signal. A CT SDM has implicit AAF and generally consumes lesser power than DT SDM. These advantages make CT SDM a good choice for wireless applications [8].

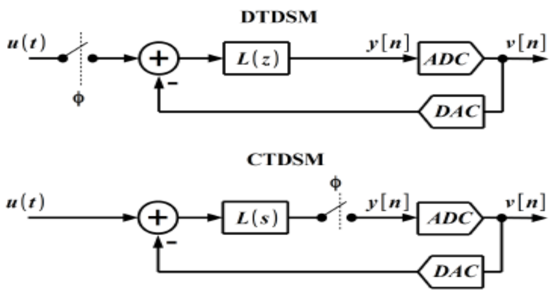


Fig. 2 Block diagram of DT and CT SDM

For a CT modulator, the sample values of the CT waveform at the input of the quantizer at each sampling instance define an exact DT impulse response. To make the DT $h_d(n)$ and CT loops equivalent, the open loop impulse responses of the discrete time loop filters, from quantizer outputs to the input of quantizer, should match the samples of the impulse response of the continuous time modulator loops [9]. That is:

$$h_d(n) = [h_{DAC}(t) * h_c(t)]|_{t=nTs} \quad (1)$$

The Laplace domain to the *z* domain mapping is established through impulse-invariant transformation (IIT) and is defined as,

$$Z^{-1}\{H_d(z)\} = L^{-1}\{H_{DAC}(s)H_c(s)\}|_{t=nTs} \quad (2)$$

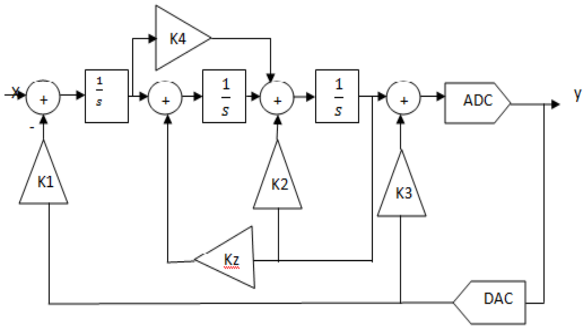


Fig. 3 Structure of used CT SDM

Loop filter can be designed by feedforward and feedback architecture. In the feed-forward structure, only one DAC is needed in the feedback path, which is more area-efficient. But signal transfer function (STF) of feedforward architecture has an out-of-band peaking at a certain frequency. This implies that at the peaking frequency the maximum stable input level is reduced by the gain of the peaking. As a result, the dynamic range is reduced and a lot of big out-of-band interferers exist.

The feedback structure [5] requires several DACs feeding back to each integrator output. The feedback filter does not suffer from significant peaking, but reduces signal swings at integrator outputs.

In wireless applications, peaking in STF of the CT modulator can effectively degrade the dynamic range of receiver. The reduced integrator swings at the output of first filter stage and STF filtering that occurred both in the feedforward and feedback architecture.As a compromise between the drawbacks of STF peaking and reduced swing, a combination of feedback and feedforward architecture has been proposed in this paper. The suggested model of architecture is shown in figure 3.

2.2 CIRCUIT LEVEL DESIGN

The circuit of the first integrator, the most critical block is designed on transistor level using 180 nm CMOS technology. The basic architecture of

Sigma Delta Modulator consists of a differential amplifier, an integrator, quantizer and a DAC in the feedback loop of the modulator. The loop filter is designed as active RC integrators. When moving from the system level to circuit level, the circuit should be realizable to implement the mathematical coefficients in system level design.

2.2.1 INTEGRATOR DESIGN

The first integrator is implemented by a fully differential two-stage amplifier [10]. In this modulator active RC integrators are chosen to realize the loop filters, the resistive load makes one-stage opamp less efficient in terms of DC gain than the two-stage opamp. So in this design, all stages employ two-stage amplifiers. The differential two-stage amplifier composes of a folded cascode opamp as the first stage and a unity-gain source follower as the second stage. The circuit schematic of the opamp is shown in figure 4. The biasing circuits are modeled by ideal voltage source in the simulation.

The values of (w/l) for each transistors were calculated using the following equations:

$$I_d = \sqrt{(\mu_n Cox(w/l)Veff)/2} \quad (3)$$

Transconductance, $gm=\sqrt{(2\mu nCox(w/l)Id)}$ (4)

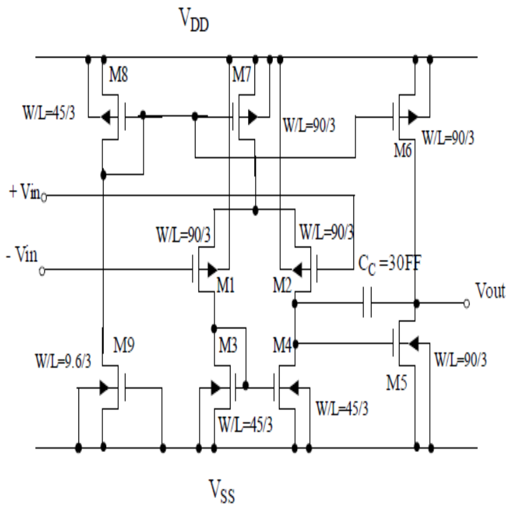


Fig. 4 Two Stage Opamp Configuration

The fully differential topology has been chosen to minimize the effects clock feed through and DC offsets and other effecs. The opmap is designed to meet the following requirements. The gain bandwidth should be atleast five times higher than switching frequency of quantizer. The DC gain should be higher and which determines the whole performance of ADC. Assuming transistors are in match, the current ratio IOUT/IREF is determined by the aspect ratio of the transistors.

III. SIMULATION RESULTS

3.1 SYSTEM LEVEL DESIGN

The proposed system level design of the continuous time third order sigma delta modulator with mixed feedback/feedforward architecture was designed in matlab/simulink. It is then compared with the discrete time implementation of second order modulator. Figure 7 and 8 shows the simulink model for the CT SDM and its corresponding SNR plot. It is observed that the continuous time implementation shows improved SNR and DR compared with discrete time counterpart. SNR and DR of about 70.5 dB and 70dB are achieved. The CT implementation could handle high bandwidth required for wireless applications.

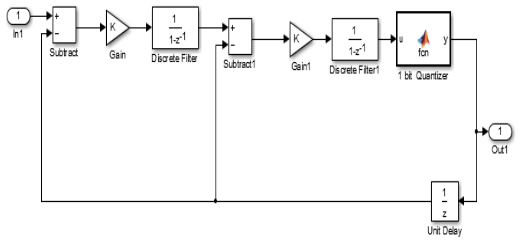


Fig. 5 Simulink model of second order DT SDM

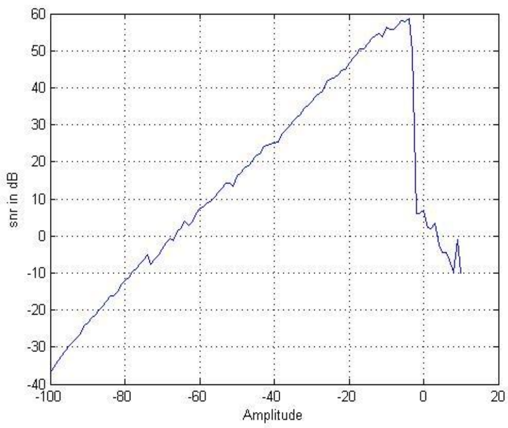


Fig. 6 SNR plot of Second order DT SDM

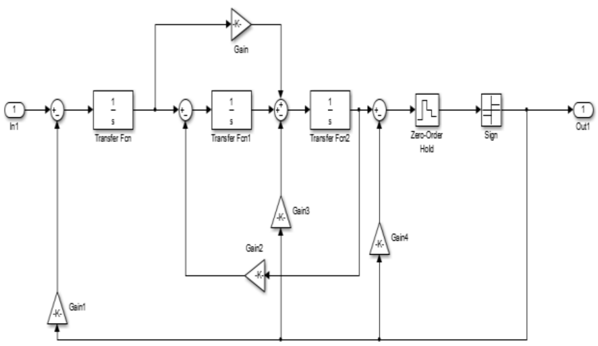


Fig. 7 Simulink model of third order CT SDM

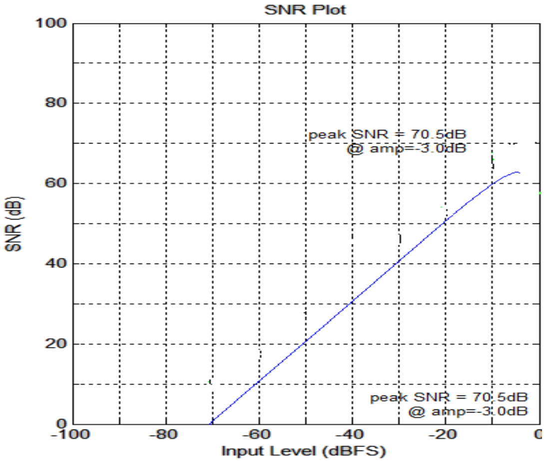
SNR and Dynamic range are calculated by using the following equations:

$$\text{SNR [dB]} = 10 \log_{10}(\text{SNR}) = 6.02N + 1.76 \text{ dB} \quad (5)$$

$$\text{DR} = \frac{3}{2}\,\frac{2L+1}{\pi^{2L}}\,\text{OSR}^{2L+1}(2^N - 1)^2 \quad (6)$$

The third order loop filter of this design is implemented with active RC operational amplifiers. The RC integrators have better linearity and larger signal swing. The coefficients in system level design are translated to the values of resistors and capacitors using:

$$\text{RC} = \frac{1}{K\,F_s} \quad (7)$$



peak SNR = 70.5dB
@ amp=-3.0dB

Fig. 8 SNR plot of Third order CT SDM

TABLE: DT &CT DSM Simulation Results

Parameter	DT	CT
SNR dB	58.7	70.5
DR dB	62	70

3.2 CIRCUIT LEVEL DESIGN

The opamp for the loop filter was designed and simulated in Cadence 180nm CMOS technology.. The simulation carried out by supplying a bias voltage of 0.6 V and power supply voltage for this circuit is only Vdd = 1.8 V was chosen. The circuit designed fully differential operational amplifier shown in figure 9 and it follows the test bench circuit. Figure 11 shows the gain plot of opamp. The DC gain of about 32 dB as been achieved with 180 nm CMOS technology.

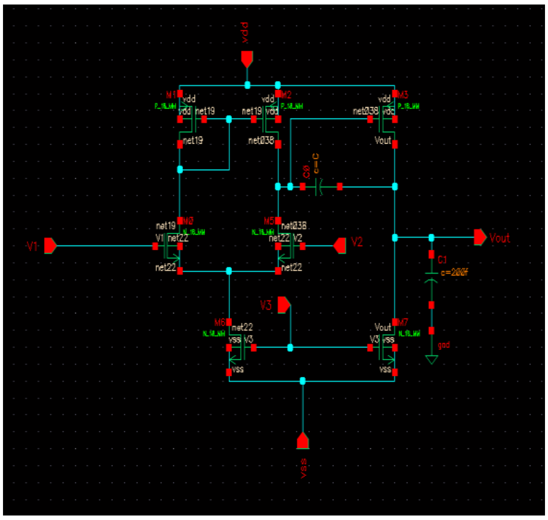


Fig. 9 Schematic of Opamp

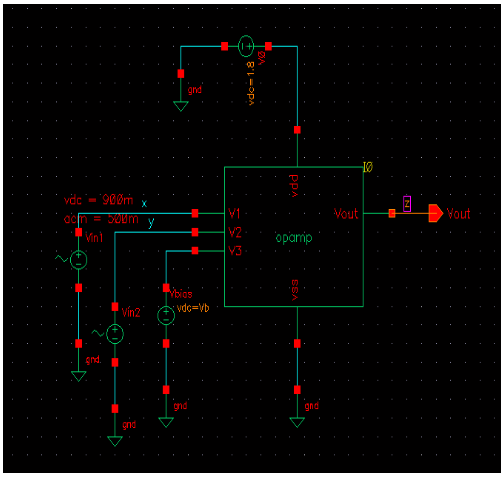


Fig. 10 Test Bench Circuit

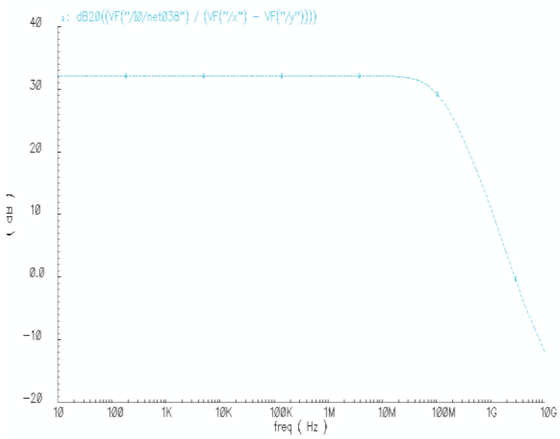


Fig. 11 Frequency Response

DC gain = 32.14 dB

-3dB gain bandwidth = 106.1 MHz

IV. CONCLUSION

A design of 3rd order continuous time sigma delta modulator for wireless application has been presented. In this work a new topology, mixed feedback/feedforward architecture is proposed for loop filter. The system level and circuit level simulations performed on matlab/simulink and cadence. The system-level simulations show that the modulator can achieve a SNR of 70.5dB, dynamic range 70dB over a signal bandwidth 20MHz. The most critical block in the modulator, which is the integrator, is designed in Cadence 180nm technology mode. An Opamp for the loop filter has been designed to achieve 32.1dB DC gain. The mixed architecture offers an increased effective dynamic range. It also improves the SNR. However, mismatch between analog and digital paths should be considered carefully.

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